

What is claimed is:

1 1. An information processing apparatus comprising:
2 first and second computer elements which execute the same
3 instructions substantially simultaneously and which are
4 substantially synchronized with each other;
5 a first memory element which is provided in said first
6 computer element and which is read and written by said first
7 computer element during a first state;
8 a second memory element which is provided in said first
9 computer element and which is written by said second computer
10 element during the first state; and
11 a control element which makes said first computer element
12 read from said second memory element during a second state.

1 2. The information processing apparatus as claimed in claim
2 1, wherein said control element makes said first computer element
3 write to said first and second memory element during the second
4 state.

1 3. The information processing apparatus as claimed in claim
2 1, wherein said control element copies the contents of said
3 second memory element to said first memory element during the
4 second state.

1 4. The information processing apparatus as claimed in claim
2 1, wherein said control element copies the contents of said
3 second memory element to said first memory element during the
4 second state in parallel with the read or write access process

5 to said second memory element.

1 5. The information processing apparatus as claimed in claim
2 4, wherein said control element copies the contents of said
3 second memory element to said first memory element unless the
4 access is present.

1 6. The information processing apparatus as claimed in claim
2 1, wherein said second state is when said first memory element
3 has uncertainty.

1 7. The information processing apparatus as claimed in claim
2 1, wherein said second state is when said first memory element
3 is updated.

1 8. The information processing apparatus as claimed in claim
2 1, wherein said second state is when said first computer element
3 is rejoined to said second computer element.

1 9. The information processing apparatus as claimed in claim
2 1, wherein said first computer element further includes at least
3 one processor; and

4 wherein said control element creates, during said second
5 state, a first route from said second memory element to said
6 first processor in response to a read access request, a second
7 route from said processor to said second memory element in
8 response to a write access request and a third route from said
9 second memory element to said first memory element unless said

10 read access request and said write access request are present.

1 10. An information processing apparatus comprising:

2 first and second computer elements which execute the same
3 instructions substantially simultaneously and which are
4 substantially synchronized with each other;

5 a first memory area which is provided in said first computer
6 element and which is written by said first computer element
7 during a first state;

8 a second memory area which is provided in said first
9 computer element and which is read and written by said second
10 computer element during the first state; and

11 a control element which makes said first computer element
12 read from said second memory area during a second state.

1 11. The information processing apparatus as claimed in claim
2 1, wherein said control element makes said first computer element
3 write to said first and second memory area during the second
4 state.

1 12. The information processing apparatus as claimed in claim
2 1, wherein said control element copies the contents of said
3 second memory area to said first memory area during the second
4 state.

1 13. The information processing apparatus as claimed in claim
2 1, wherein said control element copies the contents of said
3 second memory area to said first memory area during the second

4 state in parallel with the read or write access process to said
5 second memory area.

1 14. The information processing apparatus as claimed in claim
2 4, wherein said control element copies the contents of said
3 second memory area to said first memory area unless the access
4 is present.

1 15. The information processing apparatus as claimed in claim
2 1, wherein said second state is when said first memory area
3 has uncertainty.

1 16. The information processing apparatus as claimed in claim
2 1, wherein said second state is when said first memory area
3 is updated.

1 17. The information processing apparatus as claimed in claim
2 1, wherein said second state is when said first computer element
3 is rejoined to said second computer element.

1 18. The information processing apparatus as claimed in claim
2 1, wherein said first computer element further includes at least
3 one processor; and

4 wherein said control element creates, during said second
5 state, a first route from said second memory area to said first
6 processor in response to a read access request, a second route
7 from said processor to said second memory area in response to
8 a write access request and a third route from said second memory

9 area to said first memory area unless said read access request
10 and said write access request are present.